09/917,972

L Number	Hits	Search Text	DB	Time stamp
1	37140	ASIC	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:19
2	2326499	test equipment	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:20
3	6936	process$3 adj core$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:20
4	19386	internal adj memory	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:20
5	1351284	test routine$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:20
6	668	(internal adj memory) with (test routine$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:21
7	16176	ASIC and (test equipment)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:21
8	501	(ASIC and (test equipment)) and (process$3 adj core$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:21
9	105	((ASIC and (test equipment)) and (process$3 adj core$1)) and (internal adj memory)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:22
10	2326499	test pattern$1 with test equipment	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:22
11	105	(((ASIC and (test equipment)) and (process$3 adj core$1)) and (internal adj memory)) and (test pattern$1 with test equipment)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:22
12	2037554	arbitrated internal bus$2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:22

13	105	((((ASIC and (test equipment)) and (process$3 adj core$1)) and (internal adj memory)) and (test pattern$1 with test equipment)) and (arbitrated internal bus$2)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:23
14	37565	ASIC trst	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:23
15	814698	SIST error$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:23
16	15952	(ASIC trst) and (SIST error$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:23
17	94	((ASIC trst) and (SIST error$1)) and (((((ASIC and (test equipment)) and (process$3 adj core$1)) and (internal adj memory)) and (test pattern$1 with test equipment)) and (arbitrated internal bus$2))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:23
18	1217321	execut$3 adj self test	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:24
19	92	(((ASIC trst) and (SIST error$1)) and (((((ASIC and (test equipment)) and (process$3 adj core$1)) and (internal adj memory)) and (test pattern$1 with test equipment)) and (arbitrated internal bus$2))) and (execut$3 adj self test)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:24
20	873025	core$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:25
21	92	((((ASIC trst) and (SIST error$1)) and (((((ASIC and (test equipment)) and (process$3 adj core$1)) and (internal adj memory)) and (test pattern$1 with test equipment)) and (arbitrated internal bus$2))) and (execut$3 adj self test)) and core$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:25
22	1913616	built-in self test	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:25
23	92	(((((ASIC trst) and (SIST error$1)) and (((((ASIC and (test equipment)) and (process$3 adj core$1)) and (internal adj memory)) and (test pattern$1 with test equipment)) and (arbitrated internal bus$2))) and (execut$3 adj self test)) and core$1) and (built-in self test)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:25
24	2722320	embedded processor execut$3 test routine$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:26

25	92	((((((ASIC trst) and (SIST error$1)) and (((((ASIC and (test equipment)) and (process$3 adj core$1)) and (internal adj memory)) and (test pattern$1 with test equipment)) and (arbitrated internal bus$2))) and (execut$3 adj self test)) and core$1) and (built-in self test)) and (embedded processor execut$3 test routine$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:26
26	3795876	integrated circuit	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:26
27	92	(((((((ASIC trst) and (SIST error$1)) and (((((ASIC and (test equipment)) and (process$3 adj core$1)) and (internal adj memory)) and (test pattern$1 with test equipment)) and (arbitrated internal bus$2))) and (execut$3 adj self test)) and core$1) and (built-in self test)) and (embedded processor execut$3 test routine$1)) and (integrated circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:27
28	5551	714/724.ccls. or 714/733.ccls. or 714/734.ccls. or 714/738.ccls. or 714/742.ccls. or 714/46.ccls. or 714/30.ccls. or 714/31.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:30
29	2	((((((((ASIC trst) and (SIST error$1)) and (((((ASIC and (test equipment)) and (process$3 adj core$1)) and (internal adj memory)) and (test pattern$1 with test equipment)) and (arbitrated internal bus$2))) and (execut$3 adj self test)) and core$1) and (built-in self test)) and (embedded processor execut$3 test routine$1)) and (integrated circuit)) and (714/724.ccls. or 714/733.ccls. or 714/734.ccls. or 714/738.ccls. or 714/742.ccls. or 714/46.ccls. or 714/30.ccls. or 714/31.ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:44
30	1615	714/25.ccls. or 714/27.ccls. or 714/28.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:45
31	1	(((((((((ASIC trst) and (SIST error$1)) and (((((ASIC and (test equipment)) and (process$3 adj core$1)) and (internal adj memory)) and (test pattern$1 with test equipment)) and (arbitrated internal bus$2))) and (execut$3 adj self test)) and core$1) and (built-in self test)) and (embedded processor execut$3 test routine$1)) and (integrated circuit)) and (714/724.ccls. or 714/733.ccls. or 714/734.ccls. or 714/738.ccls. or 714/742.ccls. or 714/46.ccls. or 714/30.ccls. or 714/31.ccls.)) and (714/25.ccls. or 714/27.ccls. or 714/28.ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/25 17:45
32	1	(((((((((ASIC trst) and (SIST error$1)) and (((((ASIC and (test equipment)) and (process$3 adj core$1)) and (internal adj memory)) and (test pattern$1 with test equipment)) and (arbitrated internal bus$2))) and (execut$3 adj self test)) and core$1) and (built-in self test)) and (embedded processor execut$3 test routine$1)) and (integrated circuit)) and (714/25.ccls. or 714/27.ccls. or 714/28.ccls.)	USPAT	2004/02/25 17:46
33	1	((((((((ASIC trst) and (SIST error$1)) and (((((ASIC and (test equipment)) and (process$3 adj core$1)) and (internal adj memory)) and (test pattern$1 with test equipment)) and (arbitrated internal bus$2))) and (execut$3 adj self test)) and core$1) and (built-in self test)) and (embedded processor execut$3 test routine$1)) and ((714/724.ccls. or 714/733.ccls. or 714/734.ccls. or 714/738.ccls. or 714/742.ccls. or 714/46.ccls. or 714/30.ccls. or 714/31.ccls.) or (714/25.ccls. or 714/27.ccls. or 714/28.ccls.))	USPAT	2004/02/25 17:46